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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/787,139	06/13/2001	Honchin En	Q63452	6279

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EXAMINER	
NORRIS, JEREMY C	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 02/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/787,139	EN ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) *1-8,14-21,27-31,34-36,39 and 47* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-13,22-26,32,37,38 and 40-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of the PCB claims (9-13, 22-26, 32, 37, 38, and 40-46) in Paper No. 11 is acknowledged. Examiner agrees with the grouping of claims as enumerated by Applicants. However, Applicants have not provided any arguments as to why the separate grouping was made. Therefore, the requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 22-26, 32, 37, 38, 40-42, and 44-46 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,251,502 (hereafter Yasue).

Yasue discloses, referring to figure 1A, a printed circuit board comprising a resin insulating substrate board (3) formed with a roughened surface and, as built thereon, a conductor circuit (6) comprising at least an electroless plated film, wherein said electroless plated film has a stress of 0 to +10 kg/mm2 [claim 22].

Additionally, Yasue, discloses, referring to figure 5C, a printed circuit board comprising a resin insulating substrate board (3) formed with a roughened surface and, as built thereon, a conductor circuit (9) comprising at least an electroless plated film, wherein said electroless plated film is complementary to said roughened surface with the electroless plated film in convex areas of the roughened surface being relatively greater in thickness than said film in concave areas of said roughened surface [claim 23].

Moreover, Yasue discloses, referring to figure 5C, a printed circuit board comprising a substrate board (1) formed with a lower-layer conductor circuit (5) and, as built thereon, an upper-layer conductor circuit (9) through the intermediary of an interlayer resin insulating layer (3), with said upper-layer conductor circuit and said lower-layer conductor circuit being interconnected by via holes (8, only one shown an plurality referred to), wherein said upper-layer conductor circuit comprises at least an electroless plated film, said interlayer resin insulating layer is provided with a roughened surface, said electroless plated film is complementary to said roughened surface, and bottoms of said via holes are also provided with an electroless plated film having a thickness equal to 50 to 100° of the thickness of the electroless plated film on said interlayer resin insulating layer [claim 24].

In addition, Yasue discloses referring to figure 1A, a printed circuit board comprising a resin insulating substrate board (3) and, as built thereon, a conductor circuit (6) comprising at least an electroless plated film, wherein said electroless plated film comprises copper and at least one metal species selected from the group

consisting of nickel, iron and cobalt (see col. 14, lines 50-55) [claim 25], wherein the proportion of said at least one metal species selected from the group consisting of nickel, iron and cobalt is 0.1 to 0.5 weight % (see col. 14, lines 55-60) [claim 26].

Furthermore, Yasue discloses, referring to figure 1, a multilayer printed circuit board comprising a core board (1) having a conductor circuit and, as built over said conductor circuit, a buildup wiring layers obtainable by building up an interlayer resin insulating layer (3) and a conductor layer (6) alternately with the conductor layers being interconnected by via holes (9), wherein said core board comprises a copper-clad laminate, the conductor circuit on said core board comprises the copper foil of said copper-clad laminate and a plated metal layer, and the thickness of the conductor circuit on said core board is not greater by more than 10 um than the thickness of the conductor layer on said interlayer resin insulating layer [claim 32].

Additionally, Yasue discloses, referring to figures 3A-3I, a multilayer printed circuit board comprising a core board (1) and, as constructed on both sides thereof, a buildup wiring layers obtainable by building up an interlayer resin insulating layer (2, 3) and a conductor layer (6) alternately with said conductor layers being interconnected by via holes (13, 14), wherein said via holes are formed in the manner of plugging the through holes in plated-through holes in said core board [claim 37], wherein the through holes in said plated-through holes have a diameter of not more than 200 um (see col. 21, lines 50-55) [claim 38].

Similarly, Yasue discloses, referring to figures 3A-3I,a multilayer printed circuit board comprising a core board (1) and, as constructed on both sides thereof, a buildup

wiring layers obtainable by building up an interlayer resin insulating layer (2, 3) and a conductor layer (6) alternately with via holes (13, 9) interconnecting conductor layers wherein the via holes (9) in a lower layer are disposed immediately over the plated-through holes (13) in said core board and via holes in an upper layer are disposed immediately over said via holes in the lower layer [claim 40].

Likewise, Yasue discloses, referring to figures 3A-3I, a multilayer printed circuit board comprising a core board (1) and, as constructed on both sides thereof, a buildup wiring layers obtainable by building up an interlayer resin insulating layer (2, 3) and a conductor layer (6) alternately with via holes (9, 13) interconnecting conductor layers, wherein said plated-through holes of core board are filled with a filler (14), with the surfaces of said filler which are exposed from said plated-through holes being covered with a conductor layer provided with lower-layer via holes and upper-layer via holes being disposed immediately over said lower-layer via holes [claim 41].

In the same fashion, Yasue discloses, referring to figures 3A-3I, multilayer printed circuit board comprising a core board (1) and, as constructed on both sides thereof, a buildup wiring layers obtainable by building up an interlayer resin insulating layer (2, 3) and a conductor layer alternately with via holes (9) interconnecting conductor layers, wherein via holes in a lower layer are disposed to plug the through holes of plated-through holes in said core board, with via holes in an upper layer being disposed immediately over said via holes in the lower layer [claim 42], wherein said lower-layer via holes are filled with metal [claim 44], wherein valleys of said lower-layer via holes are filled with a

conductive paste [claim 45], wherein valleys of said lower-layer via holes are filled with a resin [claim 46].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yasue in view of US 6,217,987 (hereafter Ono).

Yasue discloses the claimed invention as described above except Yasue does not specifically state that bumps are formed immediately above said plated-through holes. However, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to provides such bumps as it is it well known in the art to attach

bumps to via holes as evidenced by Ono (see figure 1H). The motivation for doing so would have been to allow the device of Yasue to be connected to another device.

Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 4,777,078 (hereafter Miyabayashi) in view of US 5,780,143 (hereafter Shimamoto).

Miyabayashi discloses a circuit board comprising a substrate (col. 2, line 20-30) and, as built thereon, a circuit comprised of a copper film, wherein said copper film has properties that its crystallinity is such that the X-ray diffraction half-width of the plane of copper is less than 0.3 deg (see col. 6, lines 40-50). Miyabayashi does not specifically state that the variation in thickness ((maximum thickness-minimum thickness) /average thickness) of said copper film as measured over the whole surface of said substrate is not greater than 0.4 [claims 9, 11]. However, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to make the copper film to have this relative smoothness as it is well known in the art to do so, as evidenced by Shimamoto (see col. 18, lines 50-60). The motivation for doing so would have been to provide a surface suitable for surface mounting devices.

Additionally, the modified invention of Miyabayashi discloses that the copper film has an elongation of not less than 7% (see col. 5, lines 50-55) [claims 10, 13].

Similarly, Miyabayashi discloses a printed circuit board comprising a substrate formed with a conductor circuit, an interlayer resin insulating layer built thereon and a conductor circuit comprised of a copper film as built on said interlayer resin insulating layer, said interlayer resin insulating layer having vial holes by which said conductor

circuits are interconnected (see col. 7, lines 25-65), wherein said copper film has properties that its crystallinity is such that the X-ray diffraction half-width of plane of copper is less than 0.3 deg Miyabayashi does not specifically state that the variation in thickness ((maximum thickness-minimum thickness) /average thickness) of said copper film as measured over the whole surface of said substrate is not greater than 0.4 [claim 12]. However, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to make the copper film to have this relative smoothness as it is well known in the art to do so, as evidenced by Shimamoto (see col. 18, lines 50-60). The motivation for doing so would have been to provide a surface suitable for surface mounting devices.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5,055,321 Enomoto et al.,

US 5,741,575 Asai et al..

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 703-306-5737. The examiner can normally be reached on Mon.-Th., 9AM - 6:30 PM and alt. Fri. 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-0725 for regular communications and 703-308-0725 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JCSN
February 9, 2003

David A. Zarneke
AU 2827